

This is the Revision D version of the Digital8 module. The status of this project is finished.

# Digital8 Module (Revision D)

## Table of Contents

This document is also available in PDF format.

- 1. Introduction
- 2. Programming
- 3. Hardware
  - ◆ 3.1 Circuit Schematic
  - ◆ 3.2 Printed Circuit Board
- 4. Software
- 5. Issues

## 1. Introduction

The Digital8 module provides the ability to input and output 8 bits of digital data. The direction of each bit can be changed under program control.

## 2. Programming

The programmer can download a complement mask to cause any of the bits to be complemented prior to reading.

The Digital8 module supports the Interrupt Protocol. The interrupt pending bit is set whenever the the formula:

$$L \& (\sim I) \mid H \& I \mid R \& (\sim P) \& I \mid F \& P \& (\sim I)$$

is non-zero, where:

- I is the current input bits XOR'ed with the complement mask (C)
- P is the previous value of I
- L is the low mask
- H is the high mask
- R is the raising mask
- F is the falling mask

and

- $\sim$  is bit-wise complement
- $\mid$  is bit-wise OR
- $\&$  is bit-wise AND

Once the interrupt pending bit is set, it must be explicitly cleared by the user.

## Digital8 Module (Revision D)

The Digital8 module supports both the standard shared commands and the shared interrupt commands in addition to the following commands:

Command	Send/ Receive	Byte Value								Discussion
		7	6	5	4	3	2	1	0	
Read Inputs	Send	0	0	0	0	0	0	0	0	Return 8–bits of input <i>iiii iii</i> (after XOR'ing with complement mask)
	Receive	<i>i</i>	<i>i</i>	<i>i</i>	<i>i</i>	<i>i</i>	<i>i</i>	<i>i</i>	<i>i</i>	
Read Outputs	Send	0	0	0	0	0	0	0	1	Return 8–bits of the outputs <i>oooo oooo</i> (after XOR'ing with complement mask.)
	Receive	<i>o</i>	<i>o</i>	<i>o</i>	<i>o</i>	<i>o</i>	<i>o</i>	<i>o</i>	<i>o</i>	
Read Complement Mask	Send	0	0	0	0	0	0	1	0	Return 8–bits of complement mask <i>cccc cccc</i>
	Receive	<i>c</i>	<i>c</i>	<i>c</i>	<i>c</i>	<i>c</i>	<i>c</i>	<i>c</i>	<i>c</i>	
Read Direction Mask	Send	0	0	0	0	0	0	1	1	Return 8–bits of direction mask <i>dddd dddd</i>
	Receive	<i>d</i>	<i>d</i>	<i>d</i>	<i>d</i>	<i>d</i>	<i>d</i>	<i>d</i>	<i>d</i>	
Read Low Mask	Send	0	0	0	0	0	1	0	0	Return 8–bits of low mask <i>llll llll</i>
	Receive	<i>l</i>	<i>l</i>	<i>l</i>	<i>l</i>	<i>l</i>	<i>l</i>	<i>l</i>	<i>l</i>	
Read High Mask	Send	0	0	0	0	0	1	0	1	Return 8–bits of the high mask <i>hhhh hhhh</i>
	Receive	<i>h</i>	<i>h</i>	<i>h</i>	<i>h</i>	<i>h</i>	<i>h</i>	<i>h</i>	<i>h</i>	
Read Rising Mask	Send	0	0	0	0	0	1	1	0	Return 8–bits of the rising mask <i>rrrr rrrr</i>
	Receive	<i>r</i>	<i>r</i>	<i>r</i>	<i>r</i>	<i>r</i>	<i>r</i>	<i>r</i>	<i>r</i>	
Read Falling Mask	Send	0	0	0	0	0	1	1	1	Return 8–bits of the falling mask <i>ffff ffff</i>
	Receive	<i>f</i>	<i>f</i>	<i>f</i>	<i>f</i>	<i>f</i>	<i>f</i>	<i>f</i>	<i>f</i>	
Read Inputs Raw	Send	0	0	0	0	1	0	0	0	Return raw inputs <i>rrrr rrrr/Em</i> > (no XOR with complement mask)
	Receive	<i>r</i>	<i>r</i>	<i>r</i>	<i>r</i>	<i>r</i>	<i>r</i>	<i>r</i>	<i>r</i>	
Read Analog Mask	Send	0	0	0	0	1	0	0	1	Return 8 bit analog mask <i>aaaa aaaa</i>
	Receive	<i>a</i>	<i>a</i>	<i>a</i>	<i>a</i>	<i>a</i>	<i>a</i>	<i>a</i>	<i>a</i>	
Read Outputs Raw	Send	0	0	0	0	1	0	1	0	Return raw outputs <i>rrrr rrrr</i> (no XOR with complement mask)
	Receive	<i>r</i>	<i>r</i>	<i>r</i>	<i>r</i>	<i>r</i>	<i>r</i>	<i>r</i>	<i>r</i>	
Read Analog Vref	Send	0	0	0	0	1	0	1	1	Return analog Vref <i>v</i>
	Receive	0	0	0	0	0	0	0	<i>v</i>	
Reset Outputs	Send	0	0	0	1	0	0	0	0	Set all 8 bits of outputs to 0 (then XOR with complement mask).
Set Outputs	Send	0	0	0	1	0	0	0	1	Set output bits to <i>oooo oooo</i> .
	Send	<i>o</i>	<i>o</i>	<i>o</i>	<i>o</i>	<i>o</i>	<i>o</i>	<i>o</i>	<i>o</i>	
Set Complement Mask	Send	0	0	0	1	0	0	1	0	Set 8–bits of complement mask to <i>cccc cccc</i>
	Send	<i>c</i>	<i>c</i>	<i>c</i>	<i>c</i>	<i>c</i>	<i>c</i>	<i>c</i>	<i>c</i>	
Set Direction Mask	Send	0	0	0	1	0	0	1	1	Set 8–bits of direction mask to <i>dddd dddd</i> 1=input; 0=output
	Send	<i>d</i>	<i>d</i>	<i>d</i>	<i>d</i>	<i>d</i>	<i>d</i>	<i>d</i>	<i>d</i>	
Set Low Mask	Send	0	0	0	1	0	1	0	0	Set 8–bits of low mask to <i>llll llll</i>
	Send	<i>l</i>	<i>l</i>	<i>l</i>	<i>l</i>	<i>l</i>	<i>l</i>	<i>l</i>	<i>l</i>	
Set High Mask	Send	0	0	0	1	0	1	0	1	Set 8–bits of the high mask to <i>hhhh hhhh</i>
	Send	<i>h</i>	<i>h</i>	<i>h</i>	<i>h</i>	<i>h</i>	<i>h</i>	<i>h</i>	<i>h</i>	
Set Rising Mask	Send	0	0	0	1	0	1	1	0	Set 8–bits of the rising mask to <i>rrrr rrrr</i>

## Digital8 Module (Revision D)

	Send	<i>r</i>	<i>r</i>	<i>r</i>	<i>r</i>	<i>r</i>	<i>r</i>	<i>r</i>	<i>r</i>	
Set Falling Mask	Send	0	0	0	1	0	1	1	1	Set 8–bits of the falling mask to <i>ffff ffff</i>
	Send	<i>f</i>	<i>f</i>	<i>f</i>	<i>f</i>	<i>f</i>	<i>f</i>	<i>f</i>	<i>f</i>	
Set Outputs Raw	Send	0	0	0	1	1	0	0	0	Set 8–bits to <i>oooo oooo</i> with no complement mask.
	Send	<i>o</i>	<i>o</i>	<i>o</i>	<i>o</i>	<i>o</i>	<i>o</i>	<i>o</i>	<i>o</i>	
Set Analog Mask	Send	0	0	0	1	1	0	0	1	Set analog mask to <i>mmmm mmmm</i> .
	Receive	<i>a</i>	<i>a</i>	<i>a</i>	<i>a</i>	<i>a</i>	<i>a</i>	<i>a</i>	<i>a</i>	
Set Vref Mode	Send	0	0	0	1	1	0	1	<i>v</i>	Set Vref mode to <i>v</i> .
Reset Everything	Send	0	0	0	1	1	1	1	1	Reset all registers to 0 and set direction bits to 1 (input)
Set Output Bit	Send	0	0	1	0	<i>v</i>	<i>b</i>	<i>b</i>	<i>b</i>	Set output bit <i>bbbb</i> to <i>v</i>
Set Outputs Low	Send	0	1	0	0	<i>l</i>	<i>l</i>	<i>l</i>	<i>l</i>	Set low order 4–bits of Outputs to <i>llll</i> and then XOR complement mask
Set Outputs High	Send	0	1	0	1	<i>h</i>	<i>h</i>	<i>h</i>	<i>h</i>	Set high order 4–bits of Outputs to <i>hhhh</i> and then XOR complement mask
Set Direction Low	Send	0	1	1	0	<i>l</i>	<i>l</i>	<i>l</i>	<i>l</i>	Set low order 4–bits of direction to <i>llll</i> .
Set Direction High	Send	0	1	1	1	<i>h</i>	<i>h</i>	<i>h</i>	<i>h</i>	Set high order 4–bits of direction to <i>hhhh</i> .
Read Analog 8–bits	Send	1	0	0	0	<i>b</i>	<i>b</i>	<i>b</i>	<i>b</i>	Read 8–bits of analog data <i>aaaa aaaa</i> from port <i>bbb</i> .
	Receive	<i>a</i>	<i>a</i>	<i>a</i>	<i>a</i>	<i>a</i>	<i>a</i>	<i>a</i>	<i>a</i>	
Read Analog 10–bits	Send	1	0	0	0	1	<i>b</i>	<i>b</i>	<i>b</i>	Read 10–bits of analog data <i>aaaa aaaa ll00 000</i> from port <i>bbb</i> .
	Receive	<i>a</i>	<i>a</i>	<i>a</i>	<i>a</i>	<i>a</i>	<i>a</i>	<i>a</i>	<i>a</i>	
	Receive	<i>l</i>	<i>l</i>	0	0	0	0	0	0	
<u>Set Interrupt Commands</u>	Send	1	1	1	1	0	<i>c</i>	<i>c</i>	<i>c</i>	Set Interrupt Command <i>ccc</i> .
<u>Shared Commands</u>	Send	1	1	1	1	1	<i>c</i>	<i>c</i>	<i>c</i>	Execute Shared Command <i>ccc</i>

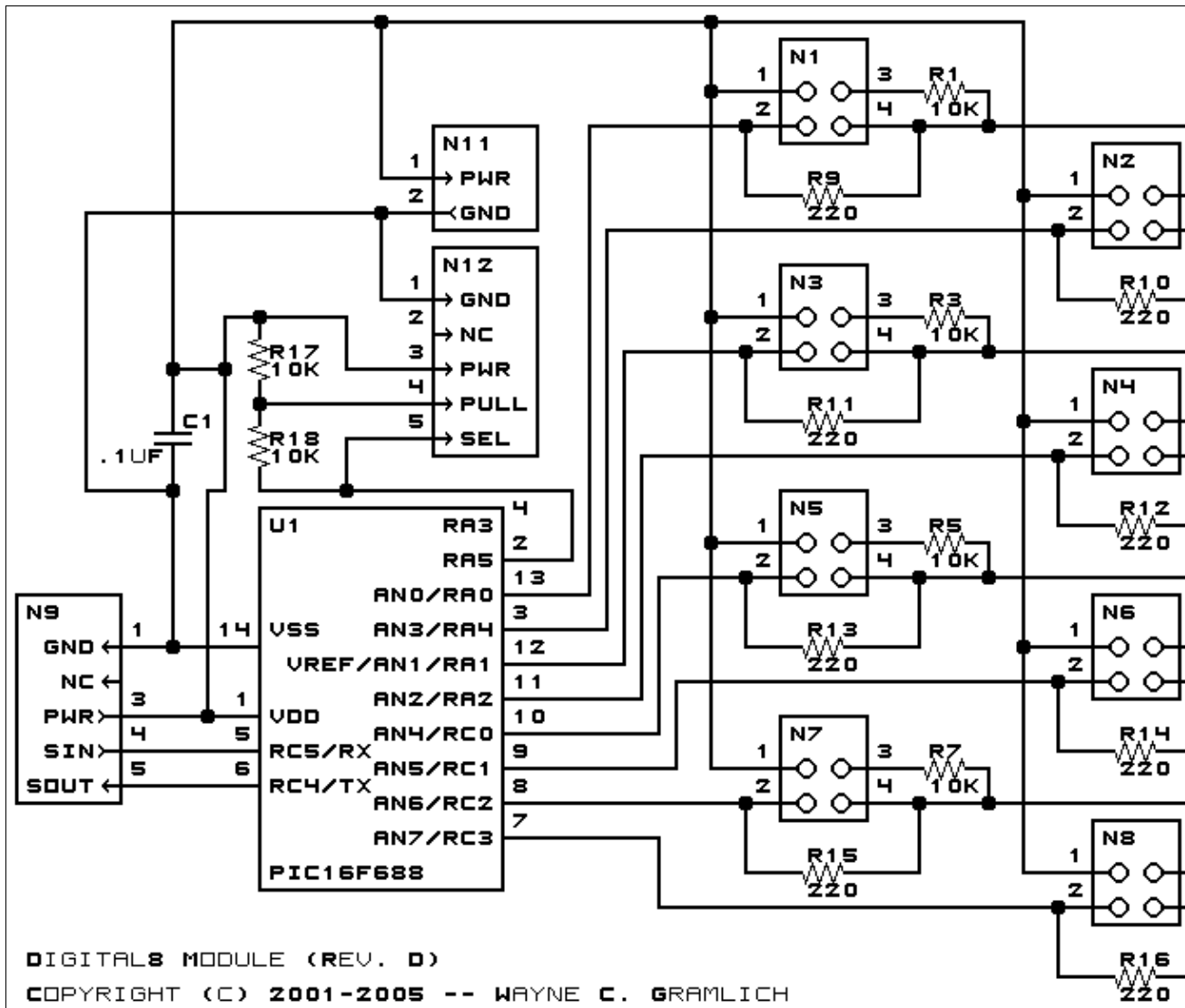
## 3. Hardware

The hardware consists of a circuit schematic and a printed circuit board.

### 3.1 Circuit Schematic

The schematic for the Digital8 module is shown below:

## Digital8 Module (Revision D)



The parts list kept in a separate file -- [digital8.ptl](#).

### 3.2 Printed Circuit Board

The printed circuit files are listed below:

[digital8\\_back.png](#)

The solder side layer.

[digital8\\_front.png](#)

The component side layer.

[digital8\\_artwork.png](#)

The artwork layer.

[digital8.gbl](#)

The RS-274X "Gerber" back (solder side) layer.

[digital8.gtl](#)

The RS-274X "Gerber" top (component side) layer.

[digital8.gal](#)

The RS-274X "Gerber" artwork layer.

*digital8.drl*

The "Excellon" NC drill file.

*digital8.tol*

The "Excellon" tool rack file.

### **3.3 Construction Instructions**

The construction Instructions are located in a separate file to be a little more printer friendly.

## **4. Software**

The Digital8 software is available as one of:

*digital8.ucl*

The  $\mu$ CL source file.

*digital8.asm*

The resulting human readable PIC assembly file.

*digital8.lst*

The resulting human readable PIC listing file.

*digital8.hex*

The resulting Intel<sup>®</sup> Hex file.

## **5. Issues**

Any fabrication issues will be listed here.

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